AMENDMENTS TO THE CLAIMS:

Please amend claim 43 and add new claims 46 and 47 as indicated below.

This listing of claims will replace all prior versions of the claims.

1. (Previously Presented) A semiconductor device comprising:

a convex semiconductor layer provided on a semiconductor substrate;

a source region and a drain region provided in the convex semiconductor layer;

a semiconductor region having an impurity concentration higher than that of a channel region provided between the source and drain regions, the semiconductor region provided between the semiconductor substrate and the source region, between the semiconductor substrate and the drain region, and between the semiconductor substrate and the channel region, respectively; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, the gate electrode applying an electric field effect to the channel region and the semiconductor region via a gate insulator, a thickness of the gate insulator being constant, and the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region.

2. (Previously Presented) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer;

a semiconductor region having an impurity concentration higher than that of a channel region provided between the source and drain regions, the semiconductor region provided

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between the semiconductor substrate and the source region, between the semiconductor substrate and the drain region and between the semiconductor substrate and the channel region, respectively;

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, the gate electrode applying an electric field effect to the channel region and the semiconductor region via a gate insulator, a thickness of a gate insulator being constant, and the side-wall gate portion being offset with respect to a part of a lower portion of the source region and a part of a lower portion of the drain region; and

a side-wall insulating film provided on a side surface of the gate electrode and the side surface of the convex semiconductor layer.

3. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a isolation film provided on a periphery of a lower portion region of the convex semiconductor layer, the position of the upper surface of the isolation film being lower than an upper surface of the convex semiconductor layer;

a source region and a drain region provided in the convex semiconductor layer, the position of the deepest portion of the source region and the position of the deepest portion of the drain region being equal to or lower than the position of the upper surface of the isolation film; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor

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layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer.

4. (Withdrawn) The device according to claim 3, wherein the source and drain regions are overlapped with the side-wall gate portion.

5. (Withdrawn) A semiconductor device comprising:

a first convex semiconductor layer provided on a substrate, the first convex semiconductor layer electrically connected to the substrate;

a second convex semiconductor layer provided on the substrate, the second convex semiconductor layer electrically connected to the substrate, the second convex semiconductor layer having the same width as the first semiconductor layer;

a first source region and a first drain region provided in the first convex semiconductor layer;

a second source region and a second drain region provided in the second convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the first convex semiconductor layer and a side surface of the second convex semiconductor layer, in an insulated state with respect to the first and second convex semiconductor layers respectively, the gate electrode applying an electric field effect to a first channel region between the first source and drain regions and a second channel region between the second source and drain regions, via at least the side surfaces of the first and second convex semiconductor layer.

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6. (Withdrawn) A semiconductor device comprising:

a first convex semiconductor layer provided on a substrate, the first convex semiconductor layer electrically connected to the substrate;

a second convex semiconductor layer provided on the substrate, the second convex semiconductor layer electrically connected to the substrate;

a first source region and a first drain region provided in the first convex semiconductor layer;

a second source region and a second drain region provided in the second convex semiconductor layer;

a first gate electrode having a first side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, the first gate electrode applying an electric field effect to a first channel region between the first source and drain regions, via at least the side surface of the first convex semiconductor layer;

a second gate electrode having a second side-wall gate portion provided over a side surface of the second convex semiconductor layer, in an insulated state with respect to the second convex semiconductor layer, the second gate electrode applying an electric field effect to a second channel region between the second source and drain regions, via at least the side surface of the second convex semiconductor layer;

a first wiring electrically connected to the first source region and the second source region;

a second wiring electrically connected to the first drain region and the second drain region; and

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a third wiring electrically connected to the first gate electrode and the second gate electrode.

7. (Withdrawn) A semiconductor device comprising:

a first convex semiconductor layer provided on a substrate;

a second convex semiconductor layer provided on the substrate;

a source region and a drain region provided in the first convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, and a gate contact portion provided over an upper surface of the second convex semiconductor layer, in an insulated state with respect to the second convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the first convex semiconductor layer.

8. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, and a upper gate portion provided over an upper surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer,

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wherein a conductive material of the side-wall gate is different from a conductive material of the upper gate portion.

9. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, and a upper gate portion provided over an upper surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer; and

a wiring being electrically connected to the upper gate portion above the upper surface of the convex semiconductor layer.

10. (Withdrawn) A semiconductor device comprising:

a first convex semiconductor layer provided on a substrate;

a second convex semiconductor layer provided on the substrate;

a first source region and a first drain region provided in the first convex semiconductor layer;

a second source region and a second drain region provided in the second convex semiconductor layer;

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a gate electrode having a side-wall gate portion provided over a side surface of the first convex semiconductor layer and a side surface of the second convex semiconductor layer, in an insulated state with respect to the first and second convex semiconductor layers respectively, the gate electrode applying an electric field effect to a first channel region between the first source and drain regions and a second channel region between the second source and drain regions, via at least the side surfaces of the first and second convex semiconductor layer; and

at least one third convex semiconductor layer electrically connected to at least either the first and the second source regions, or the first and the second drain regions.

11. (Withdrawn) A semiconductor device comprising:

a first convex semiconductor layer provided on a substrate;

a second semiconductor layer provided on the substrate;

a first source region and a first drain region of a first conductive type provided in the first semiconductor layer;

a second source region and a second drain region of a second conductive type provided in the second convex semiconductor layer, a depth of the second source region and a second drain region being deeper than the depth of the first source region and the second drain region;

a first gate electrode having a first side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, the first gate electrode applying an electric field effect to a first channel region between the first source and drain regions, via at least the side surface of the first convex semiconductor layer; and

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a second gate electrode having a second side-wall gate portion provided over a side surface of the second convex semiconductor layer, in an insulated state with respect to the second convex semiconductor layer, the second gate electrode applying an electric field effect to a second channel region between the second source and drain regions, via at least the side surface of the second convex semiconductor layer.

12. (Withdrawn) A semiconductor device comprising:

a first convex semiconductor layer provided on the substrate;

a second convex semiconductor layer provided on a substrate;

a first source region and a first drain region provided in the first convex semiconductor layer;

a second source region and a second drain region having the same conductive type as the first source region and the first drain region provided in the second convex semiconductor layer, a depth of the first source region and a depth of the second drain region being deeper than the first source region and the second drain region;

a first gate electrode having a first side-wall gate portion provided over a side surface of the first convex semiconductor layer, in an insulated state with respect to the first convex semiconductor layer, the first gate electrode applying an electric field effect to a first channel region between the first source and drain regions, via at least the side surface of the first convex semiconductor layer; and

a second gate electrode having a second side-wall gate portion provided over a side surface of the second convex semiconductor layer, in an insulated state with respect to the second convex semiconductor layer, the second gate electrode applying an electric field effect to

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a second channel region between the second source and drain regions, via at least the side surface of the second convex semiconductor layer.

13. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the gate electrode including at least a first layer and a second layer,

wherein the gate electrode uses a word line of a semiconductor memory device.

14. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the gate electrode including at least a first layer and a second layer,

wherein an upper surface of the first layer is planar and the second layer is provided on the upper surface of the first layer.

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15. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer, the gate electrode including at least a first layer and a second layer,

wherein an upper surface of the first layer has a step, the second layer is provided on the upper surface of the first layer, and an upper surface of the second layer is planar.

16. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate, the convex semiconductor having a first side surface, a second side surface opposite to the first side surface, a third side surface located between the first and second side surface, a forth side surface opposite to the third surface, and a upper surface;

a source region and a drain region provided in the convex semiconductor layer, the source region and the drain region including an electric contact portion respectively, the electric contact portion extending over a part of the first side surface, a part of the upper surface, a part of the second side surface and either of parts of the third and fourth side surfaces;

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor

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layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer.

17. (Withdrawn) A semiconductor device comprising:

a convex semiconductor layer provided on a substrate;

a source region and a drain region provided in the convex semiconductor layer; and

a gate electrode having a side-wall gate portion provided over a side surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, and a upper gate portion provided over an upper surface of the convex semiconductor layer, in an insulated state with respect to the convex semiconductor layer, the gate electrode applying an electric field effect to a channel region between the source and drain regions, via at least the side surface of the convex semiconductor layer,

wherein a gate length of the side-wall gate portion is shorter than the gate length of the upper gate portion.

18. (Withdrawn) A method of manufacturing a semiconductor device comprising:

etching a semiconductor substrate to form a convex semiconductor layer on the semiconductor substrate;

forming a gate insulating film at least on a side surface of the convex semiconductor layer;

forming a gate electrode on the gate insulating film;

forming a side-wall insulating film on a side surface of the gate electrode an on the side surface of the convex semiconductor layer; and

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introducing impurity into the convex semiconductor layer by using at least the gate electrode and the side-wall insulating film as a mask to form a source region and a drain region in the convex semiconductor layer.

19. (Withdrawn) A method of manufacturing a semiconductor device comprising:

forming an insulating film having an open hole on a semiconductor substrate;

forming a convex semiconductor layer on a semiconductor substrate exposed from the open hole;

forming a gate insulating film on at least a side surface of the convex semiconductor layer;

forming a gate electrode on the gate insulating film; and

introducing impurity into the convex semiconductor layer by using at least the gate electrode as a mask to form a source region and a drain region in the convex semiconductor layer.

20. (Withdrawn) The method according to claim 19, wherein the convex semiconductor layer is formed with the epitaxial growth method.

21. (Withdrawn) A method of manufacturing a semiconductor device comprising:

forming a convex semiconductor layer on a substrate;

forming an insulator at a periphery of the convex semiconductor layer;

forming a trench to form a side-wall gate portion in the insulator;

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forming a gate insulating film on a side surface of the convex semiconductor layer exposed at least from the trench;

forming a gate electrode having a side-wall gate portion formed in the trench; and

introducing impurity into the convex semiconductor layer by using at least the gate electrode as a mask to form a source region and a drain region in the convex semiconductor layer.

22. (Canceled)

23. (Canceled)

24. (Withdrawn) The device according to claim 1, further comprising:

a first gate insulating film provided between the side surface of the semiconductor layer and the side-wall gate portion; and

a second gate insulating film provided between an upper surface of the convex semiconductor layer and the gate electrode except for the side-wall gate portion, the second gate insulating film being thicker than the first gate insulating film.

25. (Withdrawn) The device according to claim 1, wherein the convex semiconductor layer has a tapered shape toward an upper surface of the convex semiconductor layer from the substrate.

26. (Withdrawn) The device according to claim 1, wherein a lower portion of the

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convex semiconductor layer has a tapered shape toward an upper surface of the convex semiconductor layer from the substrate.

27. (Withdrawn) The device according to claim 1, wherein a bottom corner of the convex semiconductor layer has a round shape.

28. (Withdrawn) The device according to claim 1, wherein a top corner of the convex semiconductor layer has a round shape.

29. (Withdrawn) The device according to claim 1, wherein an angle of a top corner of the convex semiconductor layer is larger than 90 degrees.

30. (Withdrawn) The semiconductor layer according to claim 1, further comprising:

an insulator provided between the substrate and the convex semiconductor layer; and

a semiconductor region provided between a bottom portion of the source region and the insulator, a bottom portion of the drain region and the insulator and the channel region and the insulator, the semiconductor region having the same conductive type as the channel region.

31. (Withdrawn) The device according to claim 30, wherein the convex semiconductor layer is amorphous silicon.

32. (Withdrawn) The semiconductor device according to claim 1, wherein the source region and the drain region includes an electric contact portion respectively, the electric contact

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portion extends over a part of the side surface of the convex semiconductor layer, an upper surface of the convex semiconductor layer and a part of another side surface of the convex semiconductor layer opposite to the side surface.

33. (Withdrawn) The device according to claim 1, further comprising:

a first gate insulating film provided between the side surface of the semiconductor layer and the side-wall gate portion; and

a second gate insulating film provided between an upper surface of the convex semiconductor layer and the gate electrode except for the side-wall gate portion, the second gate insulating film being thinner than the first gate insulating film.

34. (Withdrawn) The device according to claim 1, further comprising:

a first gate insulating film provided between the side surface of the semiconductor layer and the side-wall gate portion; and

a second gate insulating film provided between an upper surface of the convex semiconductor layer and the gate electrode except for the side-wall gate portion, and a top corner of the second gate insulating film having a round shape.

35. (Original) The device according to claim 1, wherein a distance between the source region and the drain region becomes longer toward a lower portion from an upper portion of the convex semiconductor layer.

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36. (Original) The device according to claim 1, wherein an impurity concentration of the

source region and the impurity concentration of the drain region become lower toward a lower portion from an upper portion of the convex semiconductor layer.

37. (Original) The device according to claim 1, wherein the side-wall gate portion is formed to a portion under the source region and the drain region along the side surface of the convex semiconductor layer.

38. (Original) The device according to claim 1, wherein a width of the convex semiconductor layer is smaller than 0.2 μm.

39. (Original) The device according to claim 1, wherein a width of the convex semiconductor layer is smaller than the depth of the source region and the depth of the drain region.

40. (Original) The device according to claim 1, wherein at least one of the source region and the drain region includes at least two kinds of diffusion layers, a high concentration diffusion layer having a dense impurity concentration and a low concentration diffusion layer having an impurity concentration lower than the high concentration diffusion layer.

41. (Original) The device according to claim 1, wherein the convex semiconductor layer is electrically connected to the substrate.

42. (Original) The device according to claim 1, wherein the substrate is conductive.

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43. (Currently Amended) The device according to claim 1, ~~further comprising:~~

~~a gate insulating film provided between the side-wall gate portion and the side surface of the convex semiconductor layer,~~

wherein the gate ~~insulating film is made of~~ insulator comprises an oxide including at least one of Ta, Sr, Al, ~~Si,~~ Zr, Hf, La and Ti.

44. (Previously Presented) The device according to claim 1, wherein a position of a deepest portion of the gate electrode is deeper than a position of a deepest portion of the source region and a position of a deepest portion of the drain region.

45. (Previously Presented) The device according to claim 2, wherein a position of a deepest portion of the gate electrode is deeper than a position of a deepest portion of the source region and a position of a deepest portion of the drain region.

46. (New) The device according to claim 2, wherein a width of the convex semiconductor layer is smaller than 0.2 μm.

47. (New) The device according to claim 2, wherein the gate insulator comprises an oxide including at least one of Ta, Sr, Al, Zr, Hf, La and Ti.

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